

The Honorable James L. Robart

UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF WASHINGTON  
AT SEATTLE

MICROSOFT CORPORATION, a Washington  
corporation,

Plaintiff,

v.

MOTOROLA, INC., and MOTOROLA  
MOBILITY, INC., and GENERAL  
INSTRUMENT CORPORATION,

Defendants.

CASE NO. C10-1823-JLR

MOTOROLA'S RESPONSIVE CLAIM  
CONSTRUCTION BRIEF

**HEARING DATE:**  
**March 9, 2012 at 9:00 a.m.**

MOTOROLA MOBILITY, INC., and  
GENERAL INSTRUMENT CORPORATION,

Plaintiffs/Counterclaim Defendant,

v.

MICROSOFT CORPORATION,

Defendant/Counterclaim Plaintiff.

MOTOROLA'S RESPONSIVE CLAIM CONSTRUCTION  
BRIEF  
CASE NO. C10-1823-JLR

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Pursuant to Local Rule 134 and the Court's instructions at the hearing on January 24, 2012 (ECF No. 167), Plaintiffs Motorola Mobility, Inc. and General Instrument Corporation (collectively "Motorola") submit the following brief in response to Defendant Microsoft Corporation's ("Microsoft") Opening Claim Construction Brief ("Microsoft's Brief") (ECF No. 173).

## I. INTRODUCTION

As Motorola explained in its Opening Brief, Motorola's proposed constructions are consistent with the intrinsic record of the Motorola Asserted Patents. ECF No. 174, 1:16-17. And indeed, with the exception of the term "macroblock," which is a well-known term of art incorporated into the patents, each of the disputed terms is readily understood according to its plain and ordinary meaning. Microsoft, however, ignores these plain and ordinary meanings and, instead, relies on extrinsic evidence and tortured readings of the patents to redefine simple claim language. The law is clear: claims are to be understood according to their plain meaning, and the specification is the single best guide to the proper construction of patent claims. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313-14 (Fed. Cir. 2005). Motorola's proposed constructions are consistent with these bedrock principles and should be adopted.

## II. TECHNOLOGICAL BACKGROUND

Separate and apart from the parties' claim construction disputes, Microsoft weaves into its Opening Brief several side issues that require clarification.

First, Microsoft asserts that the Motorola Asserted Patents describe in detail only encoding, not decoding, operations. ECF No. 173, 4:12-13. Not so. The patents are expressly directed to "encoding *or decoding* digital video content." *See, e.g.*, ECF No. 159-1, Ex. A at 2:52-56, 4:54-59. Indeed, decoders and decoding processes are referenced throughout the Asserted Patents' specifications. *See, e.g.*, ECF No. 159-1, Ex. A at 1:16-17, 24-32, 59-67, 2:52-60, 4:57-5:3, 15:64-16:65. In addition, the Asserted Patents' specification references "coding," which is a

1 general term that refers to both encoding and decoding. *Id.* at 7:25-46, 8:5-29, 55-65, 12:57-  
 2 13:11, 14:37-15:63.

3 Additionally, Microsoft pretends that H.264 decoding functionality is unimportant to the  
 4 accused products. ECF No. 173, 4:5-9. But Microsoft admitted prior to this litigation that H.264  
 5 was becoming an important video coding standard. Ex. AB at 134 (describing H.264 as “the most  
 6 widely accepted video coding standard”). Notably, Microsoft has not removed this “unimportant”  
 7 functionality from its products.

8 Finally, Microsoft’s argument that modern displays do not use interlaced video improperly  
 9 confuses display technology with video compression technology. ECF No. 173, 3:15-22. Modern  
 10 displays can display video content captured in interlaced format, such as the 1080i format of  
 11 HDTV broadcasts. As a result, support for interlaced content is important for today’s digital video  
 12 decoders.

### 13 III. ARGUMENT

#### 14 A. “macroblock”

15 As explained in Motorola’s Opening Brief, the term “macroblock” has a widely understood  
 16 meaning in the field of video coding—a meaning that is stated as a definition in the H.264  
 17 standard, which is incorporated by reference into the Motorola Asserted Patents. ECF No. 174, 3-  
 18 4. Specifically, a “macroblock” is “a picture portion comprising a 16×16 pixel region of luma and  
 19 corresponding chroma samples.” *Id.*

20 Microsoft, however, argues that a single statement in the specifications of the Motorola  
 21 Asserted Patents, coupled with extrinsic evidence that is unrelated to the video coding standards to  
 22 which the patents relate, suggests that any “rectangular group of pixels” is a macroblock. ECF  
 23 No. 173, 6:1-2. But Microsoft’s construction is contrary to the overwhelming weight of intrinsic  
 24 and relevant extrinsic evidence that supports Motorola’s construction, and would result in such a  
 25 broad construction that it effectively would render the term macroblock meaningless.

1 First, as explained in Motorola's Opening Brief, the claims and specifications of the  
 2 Motorola Asserted Patents consistently teach that "macroblocks" are 16x16. ECF No. 174, 3:16-  
 3 4:18; *see also, e.g.*, ECF No. 159-1, Ex. A at 3:10-28, 3:34-45, 5:57-58, 7:9-10, 7:58-67, 8:37-43,  
 4 FIGS. 2, 3, 6, 7, 8, 9, 10. The Motorola Asserted Patents also consistently distinguish between  
 5 "macroblocks" and both smaller and larger picture regions. ECF No. 174, 6:6-16; *see also, e.g.*,  
 6 ECF No. 159-1, Ex. A at 5:61-64, 7:20-23, 18:55-57. The Motorola Asserted Patents incorporate  
 7 by reference the Joint Final Committee Draft ("JFCD") of the H.264 Standard, which ***expressly***  
 8 ***defines*** "macroblock" to be 16x16. ECF No. 174, 3:19-4:1; *see also* ECF No. 160-3, Ex. N at  
 9 MS-MOTO\_1823\_00001461773. The definition in the JFCD should thus be treated as if it was  
 10 stated verbatim in the patents' specification. *LG Elecs., Inc. v. Bizcom Elecs., Inc.*, 453 F.3d 1364,  
 11 1375 (Fed. Cir. 2006) (holding that the trial court erred by failing to give proper weight to the  
 12 incorporated industry standard, which described the preferred embodiment). Thus, one of  
 13 ordinary skill reading the term "macroblock" in the context of the entire patent – and not just the  
 14 snippet Microsoft focuses on in isolation – would have attributed to it a size of 16x16.

15 Second, the prosecution history distinguishes a "macroblock" of size 16x16 from the  
 16 smaller blocks included in the macroblock. During prosecution of the '376 patent, the Examiner  
 17 cited U.S. Patent 5,504,530 ("Obikane"). Obikane defines a "macroblock" as "consisting of a  
 18 16x16 array of picture elements," and states that "within each macroblock, the image data is  
 19 arranged in the 8x8 blocks..." ECF No. 173-12, Ex. F at 3:10-30. In responding to the  
 20 Examiner's Office action regarding Obikane, Motorola distinguished "macroblock" from the  
 21 smaller blocks, stating: "The citations indicated by the Examiner (col. 3:10-30) merely discuss the  
 22 formation of a macroblock as having a plurality of smaller blocks." ECF No. 160-1, Ex. J at  
 23 MOTM\_WASH1823\_0047418.

24 Third, Microsoft's extrinsic evidence is inconsistent with the intrinsic record of the  
 25 Motorola Asserted Patents and, for that reason alone, it should be rejected. *Vitronics Corp. v.*  
 26 *Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996). Moreover, Microsoft's extrinsic

evidence does not reflect accepted usage of the term “macroblock” in the art of video coding. Specifically, Microsoft’s extrinsic evidence uses the term “macroblock” to refer to blocks that are 16×8 and 8×8 pixels. But the patents – consistent with the understanding in the field of art – refer to **blocks** of 16×8 pixels and 8×8 pixels as “smaller block sizes” and expressly distinguish them from “macroblocks,” which must be 16×16. ECF No. 159-1, Ex. A at 5:59-67, 3:10-28, 34-45. Meanwhile, the AVC-158 (Ex. B to ECF No. 173) and AVC-164 (Ex. A to ECF No. 173) proposals and U.S. Patent No. 5,878,166 (Ex. C to ECF No. 173) relied on by Microsoft were not adopted into any standards. In contrast, the MPEG video coding standards – which were adopted and one of which was incorporated by reference in the patents – consistently define “macroblocks” as being of size 16×16. ECF No. 174, 4:19-5:9.<sup>1</sup>

Fourth, Microsoft’s argument that Motorola has “no support for adding add (sic) the phrases ‘region of luma and corresponding chroma samples’ into” the construction of “macroblock,” (ECF No. 173 at 7), ignores the well-known relationship between picture elements (also known as “pixels”) and luminance (“luma”) and chrominance (“chroma”) samples. For example, the incorporated JFCD refers to “luma” and “chroma” in its express definition of “macroblock.” ECF No. 160-3, Ex. N at MS-MOTO\_1823\_00001461773.<sup>2</sup>

Finally, the cases which Microsoft cites are inapposite. For example, *Silicon Graphics, Inc. v. ATI Techs., Inc.*, 607 F.3d 784, 792-793 (Fed. Cir. 2010) fails to support Microsoft’s position because *Silicon Graphics* did not involve incorporation of an industry standard with an express definition. And, unlike the language used in the patents at issue in *Conoco* and *Edwards Sys. Tech.*, the patents here do not introduce the 16×16 size of a macroblock as a numerical range, or as taking on multiple sizes. *See Conoco, Inc. v. Energy & Env’tl. Int’l, L.C.*, 460 F.3d 1349, 1358 (Fed. Cir. 2006) (stating amount “may vary widely”); *Edwards Sys. Tech., Inc. v. Digital*

<sup>1</sup> ECF No. 174, 4-5; ECF No. 160-3, Ex. N at MS-MOTO\_1823\_00001461773 (JFCD); ECF No. 163-1, Ex. X at 9 (H.264 3/2010); Ex. AC at 3, 10, 14 (H.261); Ex. AD at 5, 21 (MPEG-2/H.262); Ex. AE at 19, 35 (MPEG 4, Part 2).

<sup>2</sup> *See also* ECF No. 173-12, Ex. F at 3:12-21 (defining macroblock in terms of picture elements (“pixels”) and its luminance (“Y”) and chrominance (“Cb” and “Cr”) components).

1 *Control Sys., Inc.*, 99 F. App'x 911, 919 (Fed. Cir. 2004) (stating a range “on the order of 25 to 50  
2 microns”). Rather, 16×16 is the sole size disclosed and is consistent with the ordinary and  
3 customary meaning of “macroblock.”

4 Accordingly, the Court should reject Microsoft’s arguments and adopt Motorola’s  
5 proposed construction of the term “macroblock.”

6 B. “decoding at least one of said plurality of smaller portions at a time...”

7 In its Opening Brief, Motorola explains how the disputed “decoding” step would be  
8 understood according to its plain and ordinary meaning by a person of ordinary skill in the art.  
9 Microsoft, however, attempts to break down this step into component terms—terms that Microsoft  
10 never proposed for separate construction. In so doing, Microsoft deviates even further from the  
11 plain and ordinary meaning of the claim.

12 1. “decoding...”

13 As explained in Motorola’s Opening Brief, “decoding” is a well-known term that carries  
14 no special meaning in the Motorola Asserted Patents. ECF No. 174, 7:18-24. Microsoft,  
15 however, argues that Motorola’s construction fails to differentiate between the claimed “decoding”  
16 step and the preamble of claim 8. ECF No. 173, 8:17-22. Not so.

17 Claim 8 recites a “method of **decoding an encoded picture...**” ECF No. 159-1, Ex. A at  
18 18:44 (emphases added). The method comprises two steps, a “decoding” step and a “using” step.  
19 Motorola thus agrees that the “decoding” step must leave something for the “using” step to  
20 perform, as part of the claimed method. Indeed, it does. The “decoding” step recites “decoding at  
21 least one of said plurality of smaller portions at a time...” In other words, the “decoding” step  
22 performs a decoding process on “smaller portions” of a picture. Those decoded smaller portions  
23 must then be used in the following “using” step to “construct a decoded picture,” thereby  
24 completing the method of decoding an encoded picture. Therefore, and contrary to Microsoft’s  
25 argument, the “decoding” step of claim 8 does not require any special construction to understand  
26 what it contributes to the overall claimed method.

1 Meanwhile, Microsoft fails to present any sound reason why “decoding” should be  
 2 understood as “removing frame coding or field coding.” As Motorola explained in its Opening  
 3 Brief and contrary to Microsoft’s interpretation, the patents’ specification teaches that removing is  
 4 involved only in encoding. The process of decoding operates “*in* a mode,” it does not remove a  
 5 mode. ECF No. 174, 8:2-18.

6 2. “at a time”

7 As noted in Motorola’s Opening Brief, the parties agreed that the language “at least one of  
 8 said plurality of smaller portions *at a time*” means “more than one macroblock *together*.” ECF  
 9 No. 174 at 7, n.5. The word “together” appears in both parties’ proposed constructions. ECF  
 10 No. 173 at 8. Now, however, Microsoft argues that Motorola’s proposed construction for the  
 11 “decoding” step somehow ignores that step’s “at a time” language, and argues that “together”  
 12 cannot include processing the claimed “smaller portion” block-by-block because such processing  
 13 was allegedly distinguished by the Examiner during prosecution. ECF No. 173 at 9-11. Microsoft  
 14 is wrong.

15 As set forth in the Motorola Asserted Patents, a smaller portion (*i.e.*, more than one  
 16 macroblock) is decoded “together” (*i.e.*, as a group) in frame coding mode or field coding mode  
 17 based on the frame/field flag that is included in the bitstream before each smaller portion. ECF  
 18 No. 159-1, Ex. A at 8:46-65 (“If the AFF is performed on pairs of macroblocks, the frame/field  
 19 flag (112) is preferably included before each pair of macroblock in the bitstream. Finally, if the  
 20 AFF is performed on a group of macroblocks, the frame/field flag (112) is preferably included  
 21 before each group of macroblocks in the bitstream”); *see also* ECF No. 161, Ex. N at MS-  
 22 MOTO\_1823\_00001461813 (“**mb\_field\_decoding\_flag**”). Because a single flag indicates the  
 23 coding mode for a smaller portion, the macroblocks of the smaller portion are treated as a unit  
 24  
 25  
 26

(*i.e.*, together) for the purposes of decoding in frame coding mode or field coding mode. This is what the claim means by “at a time.”<sup>3</sup>

Further, the Examiner did not add the language “at a time” to distinguish block-by-block processing. Obikane disclosed decoding a single macroblock, not more than one macroblock, “at a time.” ECF No. 173-12, Ex. F at 8:10-18; 9:36-42; 10:30-40 (in frame mode, selecting the data arrangement in Fig. 3(A); in field mode, selecting the data arrangement in Fig. 3(B)). Thus, the Examiner’s Amendment adding “at a time” made the claims allowable because it distinguished decoding multiple macroblocks individually (Obikane) in frame mode or field mode from decoding more than one macroblock (*i.e.*, the “smaller portion”) as a unit (*i.e.*, together) in frame mode or field mode (the Motorola Asserted Patents). By thus decoding the “smaller portion” “together” in frame mode or field mode the Motorola Asserted Patents demonstrated novel features over Obikane, which treated macroblocks independent of one another.

C. “using said plurality of decoded [smaller portions/processing blocks] to construct a decoded picture”

As explained in Motorola’s Opening Brief, no construction is necessary for this term. ECF No. 174, 10:13-14. However, if construed, Motorola’s construction more adequately addresses how the term is used in the patents. Microsoft mischaracterizes Motorola’s construction as adding a “generating” step between the “decoding” and “using” steps. ECF No. 173, 18:21-22. The claims impose no limitation on how the decoded [smaller portions/processing blocks] are used to construct a decoded picture. Microsoft’s construction does not follow the plain meaning and should therefore be rejected.

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<sup>3</sup> Decoding the macroblocks of a smaller portion “at a time” in frame mode or field mode does not mean that the macroblocks of the smaller portion must be processed simultaneously. For example, the Motorola Asserted Patents state that when coding a smaller portion comprising a macroblock pair in frame mode or field mode, the top macroblock of the pair is coded first, followed by the bottom macroblock. ECF No. 159-1, Ex. A at 8:14-18.



1 D. “wherein at least one block within [said] at least one of said plurality of smaller  
2 portions at a time is encoded in inter coding mode”

3 As Motorola explained in its Opening Brief, this “wherein” clause is descriptive of the  
4 state of the claimed “at least one block” – it is in the state of having previously been encoded in  
5 inter coded mode. It does not recite a separate “encoding” step during the claimed decoding  
6 process (which would make no sense). ECF No. 174, 9:1-15. Microsoft, however, asserts that the  
7 “use of ‘at a time’ to modify ‘is encoded’ only makes sense if ‘is encoded’ refers to the act of  
8 encoding rather than the state of having been encoded.” ECF No. 173 at 21:16-17. Not so. The  
9 term “at a time” clearly modifies “at least one of said plurality of smaller portions,” as in the  
10 related “decoding” steps of each of claims 8, 14 and 19 of the ’374 patent.

11 E. “wherein at least one motion vector is received for said at least one block within at  
12 least one of said plurality of smaller portions”

13 As explained in Motorola’s Opening Brief, the term “motion vector,” as used in this  
14 “wherein” clause refers to a value that can be used to determine the amount of motion. ECF  
15 No. 174, 11:18-12:13. Microsoft, however, contends that the specification describes a motion  
16 vector and the value that can be used to determine the amount of motion as different things. ECF  
17 No. 173, 23. The specification, however, makes clear that the latter is “the compressed bits for  
18 motion vectors.” ECF No. 159-1, Ex. A. 9:38-45.

19 Microsoft further argues that the language of claims 9 and 15 requires receiving a “motion  
20 vector” fully formed without performing a calculation. ECF No. 173, 23-24. In support of its  
21 position, Microsoft contrasts claims 9 and 15, which do not describe calculations, with claims 12  
22 and 13, which do describe calculations. *Id.* Microsoft ignores the fact that claims 12 and 13  
23 depend from claim 9, and claims 17 and 18 depend from claim 15. Therefore, claims 9 and 15  
24 must necessarily be broad enough to encompass the subject matter described in their dependent  
25 claims. *See Phillips*, 415 F.3d at 1325.

1 F. “means for...” terms

2 As explained in Motorola’s Opening Brief, and consistent with Federal Circuit precedent,  
3 each of the patents’ “means” terms must be construed such that the proper scope of the function is  
4 identified along with the corresponding structure. *Lockheed Martin Corp. v. Space Sys./Loral,*  
5 *Inc.*, 324 F.3d 1308, 1318-19 (Fed. Cir. 2003). Microsoft, however, suggests further construction  
6 of the functional language of the “means” terms is required. It is not. And Microsoft wrongly  
7 insists that the claimed structures must be defined by specific algorithms, as if they were no more  
8 than general purpose computers. Microsoft’s positions are contrary to law.

9 First, the Federal Circuit has repeatedly found, in the context of interpreting claim  
10 language pursuant to Section 112(6), that the claimed function must come from the claim  
11 language. Nothing more, nothing less. *Creo Prods., Inc. v. Presstek, Inc.*, 305 F.3d 1337, 1344  
12 (Fed. Cir. 2002).

13 Second, Microsoft’s Opening Brief relies on cases construing the structure of “means”  
14 functions implemented by general-purpose computers or microprocessors. But those cases are  
15 inapplicable because, unlike the structure here (i.e., a decoder), the *only* structure identified for  
16 performing the claimed function in those cases was a microprocessor or general purpose  
17 computer.<sup>4</sup>

18 As explained in Motorola’s Opening Brief, the structure disclosed for each of the “means”  
19 terms in the Asserted Patents is a “decoder, and equivalents thereof.” Decoders are well-known  
20 structures in the field of processing digital video content. The Motorola Asserted Patents provide  
21 a list of examples of a decoder, including a processor, an application specific integrated circuit  
22 (ASIC), a field programmable gate array (FPGA), a coder/decoder (CODEC), a digital signal  
23 processor (DSP), or some other electronic device. *See* ECF No. 159-1, Ex. A at 4:58-63. A

24  
25 <sup>4</sup> *See HTC Corp. v. IPCom GmbH & Co.*, No. 2011-1004, slip op. at 17 (Fed. Cir. Jan. 30, 2012) (“processor and  
26 transceiver”); *Aristocrat Techs. Australia v. Int’l Game Tech.*, 521 F.3d 1328, 1332-33 (Fed. Cir. 2008) (“any standard  
microprocessor”); *Harris Corp. v. Ericsson Inc.*, 417 F.3d 1241, 1254 (Fed. Cir. 2005) (“a processor”); *WMS Gaming,*  
*Inc. v. Int’l Game Tech.*, 184 F.3d 1339, 1347 (Fed. Cir. 1999) (“a microprocessor or computer”); *Timeline, Inc. v.*  
*Proclarity Corp.*, 2007 WL 1103092, at \*3, 7 (W.D. Wash. 2007) (“main process” and “driver”).

number of the examples, such as an ASIC and FPGA, are hardware devices that do not require software. While a decoder “*can* be a processor,” it is most accurately described as an “electronic device that is capable of [decoding] the stream of pictures.” Cf. ECF No. 159-1, Ex. A at 4:59-60; *see also Goss Int’l Americas, Inc. v. Graphic Mgmt. Assocs., Inc.*, 739 F. Supp. 2d 1089, 1100 (N.D. Ill. 2010) (finding “controller” to be a “known structure that is a type of special purpose computer” and noting “these controllers may not even require any algorithms at all if they consist of only circuitry to perform their specific purpose”).

G. “processing blocks”/“smaller portions”

Microsoft also argues that Motorola’s proposed constructions incorrectly distinguish between “processing blocks” and “smaller portions,” which, Microsoft asserts, mean the same thing. ECF No. 173 at 12. Microsoft is incorrect.

First, neither party has proposed that either “processing block” or “smaller portion” requires construction. Second, as explained in Motorola’s Opening Brief and further addressed above, Motorola believes that the functional language of the claimed “means” terms does not require additional construction. *Creo Prods., Inc.*, 305 F.3d at 1346.<sup>5</sup>

And, as Motorola explained, to the extent further construction of the claimed functions is required, the terms “processing block” and “smaller portion” do, in fact, have distinct definitions. ECF No. 174, 20:11-18. Thus, Microsoft’s statement equating the meaning of “smaller portions” and “processing blocks” is incorrect.

1. “means for selectively decoding...”

Microsoft asserts that Motorola fails to give proper meaning to the term “selectively” in the function of the “means for selectively decoding...” ECF No. 173, 17:10-11. Not so. Motorola included “selectively” in its definition of the claimed function.

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<sup>5</sup> Motorola addressed the functional language only briefly, so that the Court may understand Motorola’s position, in the event the Court believes further construction is required.

1 As explained in Motorola's Opening Brief, the claimed function does not require separate  
2 construction. *Creo Prods., Inc.*, 305 F.3d at 1346. And, even if it is construed further,  
3 Microsoft's proposed construction of "selectively" changes the operation of the claimed function  
4 from one of "decoding" based on a mode selection to one of "choosing." ECF No. 174, 18:12-13.  
5 Microsoft's attempts to create a "choosing" step should be rejected; Motorola's construction  
6 should be adopted.

7 IV. CONCLUSION

8 For the foregoing reasons, Motorola respectfully requests that the Court adopt Motorola's  
9 proposed constructions for each of the claim terms presently in dispute.

10 DATED this 17th day of February, 2012.

11 Respectfully submitted,

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**CERTIFICATE OF SERVICE**

I hereby certify that on this day I electronically filed the foregoing with the Clerk of the Court using the CM/ECF system which will send notification of such filing to the following:

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